AMENDMENTS (ARTICLE 34)

[Received by the Japanese Patent Office on July 28, 2003.]

1) A portion from line 11 on page 3 to line 7 on page 4 is amended in accordance with amended claims under Article 19.

Amended results are as follows.

(1) A control system comprising: a system controller comprising a bus arbiter and a non-volatile memory and having only periodically executed functions and passive functions; a bus employing a center arbitration method, from which devices can be detached and to which the detached devices can be attached again as power being supplied; and a plurality of CPU boards which execute the same processes synchronously, as devices arranged on the bus, wherein: the system controller control the system to continue processes only by periodically executed functions and passive functions of a hardware structure of the system such that when one of the CPU boards on the bus is down while accessing to the non-volatile memory, the system controller assigns the right to use the bus to other CPU board according to a requirement from the other CPU board; and even if one of the CPU board is down, the system is restored by detaching the down CPU board from the bus and attaching the CPU board to the bus again as power for the whole system being supplied.

(2) The system controller according to (1) further comprising a duplex power source system having a plurality of power sources, wherein: even if one of the CPU boards or power sources is down, the system is restored by detaching the down CPU board or the down power source from the bus and attaching the detached CPU board or the detached power source to the bus again as power for the whole system being supplied.

(3) The system controller according to (2) further comprising a duplex IO board system having a plurality of IO boards, wherein: the system controller control the system to continue processes only by periodically executed

functions and passive functions of the hardware structure of the system such that when one of the CPU boards or one of the IO boards on the bus is down while accessing to the non-volatile memory, the system controller assigns the right to use the bus to other CPU board or other IO board of the duplex IO board system according to a requirement from the other CPU board or the other IO board; and even if either one of the CPU boards, the IO boards or the power sources is down, the system is restored by detaching the down CPU board, down IO board or down power source from the bus and attaching the detached device to the bus again as power for the whole system being supplied.

(4) A system control method for controlling a control system, the control system comprising: a system controller comprising a bus arbiter and a non-volatile memory and having only periodically executed functions and passive functions; a bus employing a center arbitration method from which devices can be detached or to which the detached devices can be attached again as power being supplied; and a plurality of CPU boards which execute the same processes synchronously as devices arranged on the bus, wherein: when one of the CPU boards on the bus is down while accessing to the non-volatile memory, the system controller assigns the right to use the bus to other CPU board according to a requirement from the other CPU board so as to continue processing; and the control system is restored by detaching the down CPU board from the bus and attaching the detached CPU board to the bus again as power for the whole system being supplied.